REMARKS

Amendments

Claims 1, 6 and 33 were amended to incorporate executing simultaneous read and write operations on a first bank while accessing a second bank. The form of this language was agreed upon in the Examiner Interview of September 1, 2004, a summary of which is included herewith. Claims 3, 8 and 35 were also amended to correct for proper antecedent basis due to the changes introduced in the amendments to claims 1, 6 and 33. Applicant reserves the right to reintroduce the original subject matter in one or more continuing applications.

Claim Rejections Under 35 U.S.C. § 102

The Advisory Action maintains the rejections of the Final Office Action.

Specifically, the Advisory Action of August 24, 2004 and the Final Office Action of May 17, 2004 rejected claims 1-15 and 28-38 under 35 U.S.C. § 102(e) as being anticipated by Akaogi et al. (U.S. Patent No. 6,240,040). Applicant respectfully traverses this rejection. Applicant reserves the right to swear behind the reference Akaogi et al., but submits that claims 1-15 and 28-38 are allowable for the following reasons.

The Examiner indicated in the Examiner Interview of September 1, 2004 that claims 1-15 and 28-38 may be allowable if they were amended to specifically claim simultaneous writing to while reading from a first bank of a memory while accessing a second bank, but that another search was required. As stated above, the Applicant has amended the claims as discussed with the Examiner in the Examiner Interview to claim a non-volatile synchronous memory device that is adapted to simultaneously execute read and write operations on a first bank of the plurality of addressable banks while accessing a second bank.

The Applicant disagrees with the Examiner's assessment of Akaogi et al. as disclosing a non-volatile synchronous memory with arrays of memory cells arranged in a plurality of addressable banks, each of which may be coupled onto one with an associated output buffer to store data from the corresponding addressable bank, wherein data may be read out of the buffer

simultaneously with data being read into one of the memory banks as stated in the Final Rejection of May 17, 2004 and the Advisory Action of August 28, 2004.

The Applicant maintains that Akaogi et al. discloses an asynchronous flash memory device that has localized address decoders and dual ported global address buffers, such that it allows a write operation to occur on one bank of N addressable banks while a read operation occurs on any of the N-1 remaining banks or a read operation to occur on one bank while a write operation occurs on any of the N-1 remaining banks. *See, e.g.*, Akaogi et al., column 2, line 53 to column 3, line 10, column 3, lines 11-17 and 45-52, column 4. lines 36-49, column 5, lines 48-64, column 6, line 65 to column 7, line 26, column 9, lines 8-19 and 44-45, column 10, lines 20-24, column 16, line 53 to column 17, line 3, and column 17, lines 40-65. The Applicant also maintains that Akaogi et al. discloses global read and verify sense amplifiers and does not disclose a local read buffer coupled to each of the addressable banks to store a row of data read from the coupled memory bank. *See, e.g.*, Akaogi et al., column 7. lines 27-65, column 8, lines 1-3, and column 18, lines 5-9.

The Applicant therefore respectfully maintains that Akaogi et al. does not teach or disclose copying first data from a first array bank to a first buffer and then reading the first data from the first buffer while simultaneously writing a third data to the first array bank. The Applicant also maintains that Akaogi et al. does not include copying second data stored in a row of a second non-volatile memory cell array bank to a second buffer circuit and reading the second data from the second array bank using a second external processor coupled to the flash memory while performing a write operation to write third data to a first array bank using a first external processor.

Claim 1 recites, in part, "a plurality of bank buffers, the bank buffers and addressable banks coupled one to one, wherein each of the plurality of bank buffers is adapted to store data from a row of memory cells contained in its corresponding addressable bank of the plurality of addressable banks and wherein the non-volatile synchronous memory device is adapted to simultaneously execute read and write operations on a first bank of the plurality of addressable banks while accessing a second bank." As stated above, Akaogi et al. does not teach or disclose simultaneously executing read and write operations on a first bank of the plurality of addressable banks while accessing a second bank or a plurality of bank buffers and a plurality of addressable

banks coupled one to one. Therefore, Akaogi et al. does not teach or disclose all elements of claim 1.

Claim 6 recites, in part, "a plurality of bank buffers, the bank buffers and addressable banks coupled one to one, wherein each of the plurality of bank buffers is adapted to store data from a row of memory cells contained in its corresponding addressable bank of the plurality of addressable banks and wherein the non-volatile synchronous memory device is adapted to simultaneously execute read and write operations on a first bank of the plurality of addressable banks while executing a read, write, or erase operation on a second bank." As stated above, Akaogi et al. does not teach or disclose simultaneously executing read and write operations on a first bank of the plurality of addressable banks while executing a read, write, or erase operation on a second bank, or a plurality of bank buffers and a plurality of addressable banks coupled one to one. Therefore, Akaogi et al. does not teach or disclose all elements of claim 6.

Claim 33 recites, in part, "a plurality of bank buffers, the bank buffers and addressable banks coupled one to one, wherein each of the plurality of bank buffers is adapted to store data from a row of memory cells contained in its corresponding addressable bank of the plurality of addressable banks and wherein the flash memory device is adapted to simultaneously execute read and write operations on a first bank of the plurality of addressable banks while executing an access of a second bank." As stated above, Akaogi et al. does not teach or disclose simultaneously executing read and write operations on a first bank of the plurality of addressable banks while executing an access on a second bank, or a plurality of bank buffers and a plurality of addressable banks coupled one to one. Therefore, Akaogi et al. does not teach or disclose all elements of claim 33.

Claim 11, recites copying first data stored in a row of a first non-volatile memory cell array bank to a first buffer circuit using control circuitry of the memory, copying second data stored in a row of a second non-volatile memory cell array bank to a second buffer circuit using the control circuitry, performing a write operation to write third data to the first array bank using a first external processor coupled to the flash memory, reading the first data from the first buffer circuit using the first processor while performing the write operation, and reading the second data from the second array bank using a second external processor coupled to the flash memory while performing the write operation. As stated above, Akaogi et al. does not teach or disclose

copying first data from a first array bank to a first buffer and then reading the first data from the first buffer while simultaneously writing a third data to the first array bank and reading a second data from a second array bank. Therefore, Akaogi et al. does not teach or disclose all elements of claim 11.

Applicant respectfully contends that claims 1, 6, 11 and 33 have been shown to be patentably distinct from the cited reference. As claims 2-5, 7-10, 12-15, 28-32 and 34-38 depend directly or indirectly from independent claims 1, 6, 11 and 33, respectively, they are also considered to be in condition for allowance. Accordingly, Applicant respectfully requests withdrawal of the rejection under 35 U.S.C. § 102(e) and allowance of claims 1-15 and 28-38.

Double Patenting Rejection

The Examiner provisionally rejected claims 1-11, 28-31 and 33-38 under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-23 of co-pending U. S. Patent Application Serial No. 09/628,184 (the '184 application). Applicant respectfully traverses this rejection.

The Examiner had previously rejected claims 1-15 and 28-38 under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-23 of the co-pending '184 application in the Advisory Action mailed August 24, 2004. In the present Advisory Action mailed August 24, 2004, the Examiner withdrew the double patenting rejection of claims 11-15 and 32, and affirmed the rejection of claims 1-10, 28-31 and 33-38 under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-23 of the co-pending '184 application. The Examiner further stated in regards to the double patenting rejection that claims 1-10, 28-31 and 33-38 "contain no limitation that any of the banks being read from and written to must include a SAME bank being read and written."

As stated above, the Applicant has amended claims 1, 6 and 33 to claim a non-volatile synchronous memory device that is adapted to simultaneously execute a read and a write operation on a first bank of the plurality of addressable banks while accessing a second bank, as was discussed in the Examiner Interview of September 1, 2004. Applicant respectfully maintains that the '184 application does not teach or suggest simultaneously executing a read and

a write operation on a first bank while accessing a second bank. The Applicant also respectfully maintains that the '184 application does not teach or suggest individual bank read buffers coupled one to one with each memory bank. The Applicant therefore maintains that '184 application does not teach or suggest all elements of claims 1, 6 and 33.

Therefore, claims 1, 6 and 33 of the present application are patentably distinct from claims 1-23 of the '184 application because claims 1, 6 and 33 of the present application require non-obvious limitations not included in claims 1-23 of the '184 application. As claims 2-5, 7-10, 28-31 and 34-38 depend from and further define claims 1, 6 and 33, respectively, they are also considered to be in condition for allowance. The Applicant therefore respectfully requests that the rejection of claims 1-10, 28-31 and 33-38 under the judicially created doctrine of obviousness-type double patenting be withdrawn and claims 1-10, 28-31 and 33-38 allowed.

CONCLUSION

In view of the above remarks, Applicant respectfully submits that the claims are in condition for allowance and requests reconsideration of the application and allowance of the claims.

If the Examiner has any questions or concerns regarding this application, please contact the undersigned at (612) 312-2207.

Respectfully submitted,

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